

AMI

AMI Hi-Flex BIOS

SIS Rabbit

User's Guide

MAN386DXSIS  
January 27, 1992

© Copyright 1992 American Megatrends Inc.  
All rights reserved.  
American Megatrends Inc.  
6145-F Northbelt Parkway  
Norcross, GA 30071

This publication contains proprietary information which is protected by copyright. No part of this publication may be reproduced, transcribed, stored in a retrieval system, translated into any language or computer language, or transmitted in any form whatsoever without the prior written consent of the publisher, American Megatrends, Inc.

### **Limited Warranty**

Buyer agrees if this product proves to be defective, that American Megatrends, Inc. (hereafter referred to as AMI) is only obligated to replace or refund the purchase price of this product at AMI's discretion. AMI shall not be liable in tort or contract for any loss or damage, direct, incidental or consequential. Please see the AMI Warranty Registration Card shipped with this product for full warranty details.

### **Limitations of Liability**

In no event shall AMI be held liable for any loss, expenses, or damages of any kind whatsoever, whether direct, indirect, incidental, or consequential, arising from the design or use of this product or the support materials provided with the product.

### **Trademarks**

AMI acknowledges the following trademarks:

Intel and i386 are registered trademarks of Intel Corporation.

MS-DOS, Xenix, and Microsoft are registered trademarks of Microsoft Corporation.

Weitek is a registered trademark of Weitek Corporation.

IBM, AT, VGA, OS/2, and EGA are registered trademarks of International Business Machines Corporation. XT and CGA are trademarks of International Business Machines Corporation.

## Table of Contents

### **Chapter 1 Introduction 1**

### **Chapter 2 Advanced CMOS Setup 3**

### **Chapter 3 Advanced Chip Set Setup 5**

Cache Scheme	7
Cache Size Select	7
Cache Write Wait State	7
C0000 -> C7FFF Cacheable	7
Size of Non-Cacheable Area	7
Non-Cacheable Start Address	7
Allocation, Non-Cached Area	8
DRAM RAS Pre-Charge Time	8
DRAM Write CAS Wait State	8
DRAM Read CAS Wait State	8
Keyboard Controller Clock	8
DMA Clock Select	8
8-Bit AT Cycle Wait State	8
16-Bit AT Cycle Wait State	9
Bus Clock Select	9
I/O Recover Time	9
Fast CPU Reset Option	9
Fast Reset Delay Select	9
CPU Cycle Address Hold Time	9

### **Chapter 4 CMOS Map 11**

Extended CMOS RAM	15
-------------------	----

### **Index 17**

## Preface

### To the OEM Reader

The AMI Hi-Flex BIOS is a state of the art product which includes major engineering innovations. The AMI Hi-Flex BIOS can be easily configured by the OEM, system integrator, or VAR building systems that include the AMI BIOS through the AMI BIOS Configuration Program (AMIBCP). See the *AMIBCP User's Guide* for detailed information about AMIBCP.

This manual was written for the OEM. It is the purpose of this manual to assist in preparing the AMI BIOS for the SIS Rabbit chip set for use in your new system.

This manual is not meant to be read by the computer owner who purchases a computer with the AMI Hi-Flex BIOS. It is assumed that the computer manufacturer will use this manual as a sourcebook of information, and that parts of this manual will be included in the computer owner's manual.

It is also assumed that the OEM, VAR, or system integrator that is reading this manual has also licensed the right to use the AMI BIOS technical documentation.

### AMI Technical Support

If an AMI Hi-Flex BIOS board fails to operate as described or you need more information, call the AMI technical support staff at 404-263-8181. Make sure you have the following information before calling AMI technical support:

- Serial number and revision number of the BIOS
- System BIOS reference number
- A clear description of the problem.

### Acknowledgments

This manual was written and edited by Paul Narushoff and Robert Cheng. The writers gratefully acknowledge the assistance of the AMI BIOS engineers.

### BIOS File

This manual is based on AMI BIOS file SISD3DXP.

# Chapter 1

## Introduction

### Overview

The BIOS is the basic input output system used in all IBM® PC-, XT™-, AT®-, and PS/2®- compatible computers. The AMI Hi-Flex BIOS is a high-quality example of a system BIOS.

### **Configuration Data**

AT-Compatible systems, also called ISA (Industry Standard Architecture) systems, and EISA (Extended Industry Standard Architecture) systems must have a place to store system information when the computer is turned off. The original IBM AT had 64 bytes of non-volatile memory storage in CMOS RAM. All AT-Compatible systems have at least 64 bytes of CMOS RAM, which is usually part of the Real Time Clock. Many systems have 128 bytes of CMOS RAM.

EISA systems have at least 4 KB of additional CMOS RAM to store EISA configuration information.

### **How Data Is Configured**

The AMI Hi-Flex BIOS provides a BIOS Setup utility in ROM that is accessed by pressing <Del> at the appropriate time during system boot. Setup is used to set configuration data in CMOS RAM.

## Overview, Continued

### Types of Setup

There are three types of Setup in the AMI Hi-Flex BIOS:

Types of Setup	Description
Standard CMOS Setup	Set time, date, hard disk type, types of floppy drives, monitor type, and if keyboard is installed. See the <i>AMI Hi-Flex BIOS User's Guide</i> .
Advanced CMOS Setup	Set Typematic Rate and Delay, Above 1 MB Memory Test, Memory Test Tick Sound, Hit <Del> Message Display, System Boot Up Sequence, and many others. See the <i>AMI Hi-Flex BIOS User's Guide</i> .
Advanced Chip Set Setup	Set chip set-specific options and features. See the <i>AMI Hi-FLEX BIOS User's Guide</i> .
Power Management	Set options to conserve battery power in laptop computers. There is no Power Management Setup in the AMI BIOS for the SIS 386DX Chip Set.
Peripheral Setup	Set options for configuring onboard controllers for peripherals such as floppy drives, hard disk drives, parallel ports, serial ports, etc. There is no Peripheral Setup in the AMI BIOS for the SIS 386DX Chip Set.

### Reference

Standard CMOS Setup and the standard Advanced CMOS Setup options are described in the *AMI Hi-Flex BIOS User's Guide*. Advanced Chip Setup for the AMI BIOS for the SIS Rabbit chip set is described in this manual.

# Chapter 2

## Advanced CMOS Setup

### Overview

#### **Default Settings**

Every option in the AMI BIOS Setup utility contains two default values: a power-on default and the BIOS Setup default value.

#### **The Power-on Defaults**

The power-on default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance characteristics.

#### **Setup Defaults**

The BIOS Setup default values provide optimum performance settings for all devices and system features.



## SIS Rabbit Advanced CMOS Options

See the following screen for a display of the SIS Rabbit Advanced CMOS Setup screen. In addition to the standard options, documented in the AMI Hi-Flex BIOS User's Guide, the following options are provided and are described in this chapter:

# Chapter 3

## Advanced Chip Set Setup

### Overview

This chapter describes the Advanced Chip Set Setup options for the AMI Hi-Flex BIOS for the SIS Rabbit Chip Set from Silicon Integrated Systems.

Refer to the documentation provided by the chip set manufacturer for additional assistance in understanding specific chip set options.

## Default Settings

Every option in the AMI BIOS Setup utility contains two default values: a power-on default and the BIOS Setup default value.

### **The Power-on Defaults**

The power-on default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance characteristics.

### **Setup Defaults**

The BIOS Setup default values provide optimum performance settings for all devices and system features.

### **Configuring Advanced Chip Set Options**

The OEM can choose the options that are included in the Advanced CMOS and Advanced Chip Set Setup part of the AMI Setup utility through the AMI BCP. See the *AMI BCP User's Guide* for additional information.

## Advanced Chip Set Setup Options

### **Cache Scheme**

The settings are External or Internal. The BIOS and Power-on defaults are External.

### **Cache Size Select**

The settings are 32 KB, 64 KB, 128 KB, or 256 KB. The BIOS and Power-on defaults are 32 KB.

### **Cache Write Wait State**

The settings are 0 Wait State or 1 Wait State. The BIOS default is 0 Wait State. The Power-on default is 1 Wait State.

**C0000 -> C7FFF Cacheable**  
**C8000 -> CFFFF Cacheable**  
**D0000 -> D7FFF Cacheable**  
**D8000 -> DFFFF Cacheable**  
**E0000 -> FFFFF Cacheable**

The settings are Enabled or Disabled. The BIOS default is Enabled for C0000-C7FFF and E0000-FFFFF and Disabled for all others. The Power-on default is Disabled.

### **Size of Non-Cacheable Area**

The settings are 256 KB, 512 KB, 1 MB, 2 MB, or 4 MB. The BIOS and Power-on defaults are 256 KB.

### **Non-Cacheable Start Address**

The starting address of the non-cacheable area is based on the block size. The BIOS and Power-on defaults are Disabled.

## Advanced Chip Set Setup Options, Continued

### **Allocation, Non-Cached Area**

This option selects whether the non-cacheable area applies to the onboard system memory or the AT Bus. The settings are Sys DRAM or AT Bus. The BIOS and Power-on defaults are Sys DRAM.

### **DRAM RAS Pre-Charge Time**

The settings are 3 T or 2 T. The BIOS and Power-on defaults are 2 T.

### **DRAM Write CAS Wait State**

The settings are 0 Wait State or 1 Wait State. The BIOS default is 0 Wait State. The Power-on default is 1 Wait State.

### **DRAM Read CAS Wait State**

The settings are 2 Wait States or 3 Wait States. The BIOS default is 2 Wait States. The Power-on default is 3 Wait State.

### **Keyboard Controller Clock**

The settings are 7.159 MHz, OSCLK/4, OSCLK/6, or OSCLK/8. The BIOS and Power-on defaults are 7.159 MHz.

### **DMA Clock Select**

The settings are 7.159 MHz, 4.773 MHz, or BUSCLK. The BIOS and Power-on defaults are 7.159 MHz.

### **8-Bit AT Cycle Wait State**

The settings are 4 Wait States or 5 Wait States. The BIOS default is 4 Wait States. The Power-on default is 5 Wait States.

## Advanced Chip Set Setup Options, Continued

### **16-Bit AT Cycle Wait State**

The settings are 1 Wait State or 2 Wait States. The BIOS default is 1 Wait State. The Power-on default is 2 Wait States.

### **Bus Clock Select**

The settings are OSCLK/5, OSCLK/6, OSCLK/8, or OSCLK/16. The BIOS and Power-on defaults are OSCLK/5.

### **I/O Recover Time**

This option sets the recover time for 8-bit and 16-bit bus. The settings are 6,2BCLK, 2,2BCLK, 12,4BCLK, or 12,2BCLK. The BIOS and Power-on defaults are 6,2 BCLK.

### **Fast CPU Reset Option**

The settings are Enabled or Disabled. The BIOS and Power-on defaults are Disabled.

### **Fast Reset Delay Select**

The settings are 2  $\mu$  or 4  $\mu$ s. The BIOS and Power-on defaults are 2  $\mu$ s.

### **CPU Cycle Address Hold Time**

The settings are 2-3 OCLK or 6-7 OCLK. The BIOS and Power-on defaults are 2-3 OCLK.

# Chapter 4

## CMOS Map

A map of CMOS RAM as configured by the AMI SIS Rabbit BIOS is shown in the following table.

CMOS Location	Description
00h-0Fh	Standard IBM AT compatible RTC and Status Register data definitions.
10h	Floppy Drive Type Bits 7-4 Drive A: Type 0 No Drive 1 360 KB Drive 2 1.2 MB Drive 3 720 KB Drive 4 1.44 MB Drive 5-16 Reserved Bits 3-0 Drive B: Type (bit settings same as A)
11h	Keyboard Typematic Data Bit 7 Enable Typematic (1 = On) Bits 6-5 Typematic Delay 00b 250 ms 01b 500 ms 10b 750 ms 11b 100 ms Bits 4-0 Typematic Rate 0 - 300 8 - 159 16 - 75 24 - 37 1 - 267 9 - 133 17 - 67 25 - 33 2 - 240 10 - 120 18 - 60 26 - 30 3 - 218 11 - 109 19 - 55 27 - 27 4 - 200 12 - 100 20 - 50 28 - 25 5 - 185 13 - 92 21 - 46 29 - 23 6 - 171 14 - 86 22 - 43 30 - 21 7 - 160 15 - 80 23 - 40 31 - 20
12h	Hard Disk Data Bits 7-4 Hard Disk Drive C: Type 0 No drive 1-14 Hard drive Type 1-14 16 Hard Disk Type 16-255 (actual Hard Drive Type is in CMOS RAM 1Ah) Bits 3-0 Hard Disk Drive D: Type (Same as C:)
13h	Advanced Setup Options Bit 7 Mouse Enabled (1 = On) Bit 6 Test Memory above 1 MB (1 = On) Bit 5 Memory Test Tick Sound (1 = On) Bit 4 Memory Parity Error Check (1 = On) Bit 3 Press <Esc> to Disable Memory Test (1 = On) Bit 2 User-Defined Hard Disk (1 = On) Bit 1 Wait for <F1> Message if Error (1 = On) Bit 0 Turn Num Lock Off at boot (1 = On)
14h	Equipment Byte

	Bits 7-6 Number of Floppy Drives 00b 1 Drive 01b 2 Drives 10b-11b Reserved Bits 5-4 Monitor Type 00b Not CGA or MDA 01b 40x25 CGA 10b 80x25 CGA 11b MDA (Monochrome) Bit 3 Display Enabled (1 = On) Bit 2 Keyboard Enabled (1 = On) Bit 1 Math coprocessor Installed (1 = On) Bit 0 Floppy Drive Installed (0 = On)
15h	Base Memory (in 1K increments), Low Byte
16h	Base Memory (in 1K increments), High Byte
17h	Extended Memory (in 1K increments), Low Byte
18h	Extended Memory (in 1K increments), High Byte (Max 15 MB)
19h	Hard Disk C: Drive Type 0-15 Reserved 16-255 Hard Drive Type 16-255
1Ah	Hard Disk D: Drive Type (Same as Drive C: above)
1Bh	User-Defined Drive C: - # of Cylinders, Low Byte
1Ch	User-Defined Drive C: - # of Cylinders, High Byte
1Dh	User-Defined Drive C: - Number of Heads
1Eh	User-Defined Drive C: - Write Precompensation Cylinder, Low Byte
1Fh	User-Defined Drive C: - Write Precompensation Cylinder, High Byte
20h	User-Defined Drive C: - Control Byte (80h if # of heads is equal or greater than 8)
21h	User-Defined Drive C: - Landing Zone, Low Byte
22h	User-Defined Drive C: - Landing Zone, High Byte
23h	User-Defined Drive C: - # of Sectors
24h	User-Defined Drive D: - # of Cylinders, Low Byte
25h	User-Defined Drive D: - # of Cylinders, High Byte
26h	User-Defined Drive D: - Number of Heads
27h	User-Defined Drive D: - Write Precompensation Cylinder, Low Byte
28h	User-Defined Drive D: - Write Precompensation Cylinder, High Byte
29h	User-Defined Drive D: - Control Byte (80h if # of heads is equal or greater than 8)
2Ah	User-Defined Drive D: - Landing Zone, Low Byte
2Bh	User-Defined Drive D: - Landing Zone, High Byte
2Ch	User-Defined Drive D: - # of Sectors
2Dh	Configuration Options Bit 7 Weitek Installed (1 = On) Bit 6 Floppy Drive Seek - turn off for fast boot Bit 5 Boot Order 0 - Drive C.; then A: 1 - Drive A.; then C: Bit 4 Boot Speed (0 - Low; 1 - High) Bit 3 External Cache Enable(1 = On)



	Bit 2 Internal Cache Enable (1 = On) Bit 1 Use Fast Gate A20 after boot (1 = On) Bit 0 Turbo Switch (1 = On)
2Eh	Standard CMOS Checksum, High Byte
2Fh	Standard CMOS Checksum, Low Byte
30h	Extended Memory, Low Byte
31h	Extended Memory, High Byte (Maximum 15 MB)
32h	Century Byte (BCD value for the century)
33h	Information Flag Bit 7 128K Bits 6-0 Reserved
34h	Shadowing Bits 7-6 Password 00b Disable 10b Reserved 01b Set 11b Boot Bit 5 C8000h Shadow Adaptor ROM (Bit 1 = On) Bit 4 CC000h Shadow Adaptor ROM (Bit 1 = On) Bit 3 D0000h Shadow Adaptor ROM (Bit 1 = On) Bit 2 D4000h Shadow Adaptor ROM (Bit 1 = On) Bit 1 D8000h Shadow Adaptor ROM (Bit 1 = On) Bit 0 DC000h Shadow Adaptor ROM (Bit 1 = On)
35h	Shadowing Bit 7 E0000h Shadow Adaptor ROM (Bit 1 = On) Bit 6 E4000h Shadow Adaptor ROM (Bit 1 = On) Bit 5 E8000h Shadow Adaptor ROM (Bit 1 = On) Bit 4 EC000h Shadow Adaptor ROM (Bit 1 = On) Bit 3 F0000h Shadow System ROM (Bit 1 = On) Bit 2 C0000h Shadow Video ROM (Bit 1 = On) Bit 1 C4000h Shadow Video ROM (Bit 1 = On) Bit 0 Reserved
36h-37h	Reserved
38h-3Dh	Encrypted Password
3Eh	Extended CMOS Checksum, High Byte (includes 34h - 3Dh)
3Fh	Extended CMOS Checksum, Low Byte (includes 34h - 3Dh)

## Extended CMOS RAM

CMOS Location	Description
40h	Bits 6-5 Cache Size Select Bit 4 Cache Write Wait State Bit 2 DRAM RAS Pre-Charge Time Bit 0 E0000 -> FFFFF Cacheable
41h	Bit 7 Cache Scheme Bit 5 DRAM Write CAS Wait State Bit 4 DRAM Read CAS Wait State
42h	Bit 3 D8000 -> DFFFF Cacheable Bit 2 D0000 -> D7FFF Cacheable Bit 1 C8000 -> CFFFF Cacheable Bit 0 C0000 -> C7FFF Cacheable
43h	Bits 7-2 Non-Cacheable Start Address
44h	Bits 2-0 Size of Non-Cacheable Area
45h	Bit 0 Allocation, Non-Cached Area
46h	Bits 7-6 Keyboard Controller Clock Bits 5-4 DMA Clock Select Bit 3 8-Bit AT Cycle Wait State Bit 2 16-Bit AT Cycle Wait State Bits 1-0 Bus Clock Select
47h	Bits 7-6 I/O Recover Time Bit 4 Fast CPU Reset Option Bit 3 CPU Cycle Address Hold Time Bit 1 Fast Reset Delay Select
48h-7Fh	Reserved

# Index

16-Bit AT Cycle Wait State 9  
8-Bit AT Cycle Wait State 8  
Advanced Chip Set Setup Options 5  
Allocation, Non-Cacheable Area 8  
AMI BCP 6  
BCP 6  
Bus Clock Select 9  
C0000 -> C7FFF Cacheable 7  
Cache Scheme 7  
Cache Size Select 7  
Cache Write Wait State 7  
CMOS Map 11  
CPU Cycle Address Hold Time 9  
Default Settings 6  
DMA Clock Select 8  
DRAM RAS Pre-Charge Time 8  
DRAM Read CAS Wait State 8  
DRAM Write CAS Wait State 8  
Extended CMOS RAM 15  
Fast CPU Reset Option 9  
Fast Reset Delay Select 9  
I/O Recover Time 9  
Keyboard Controller Clock 8  
Non-Cacheable Start Address 7  
Power-on default 6  
Setup Defaults 6  
Size of Non-Cacheable Area 7